FIG. 1

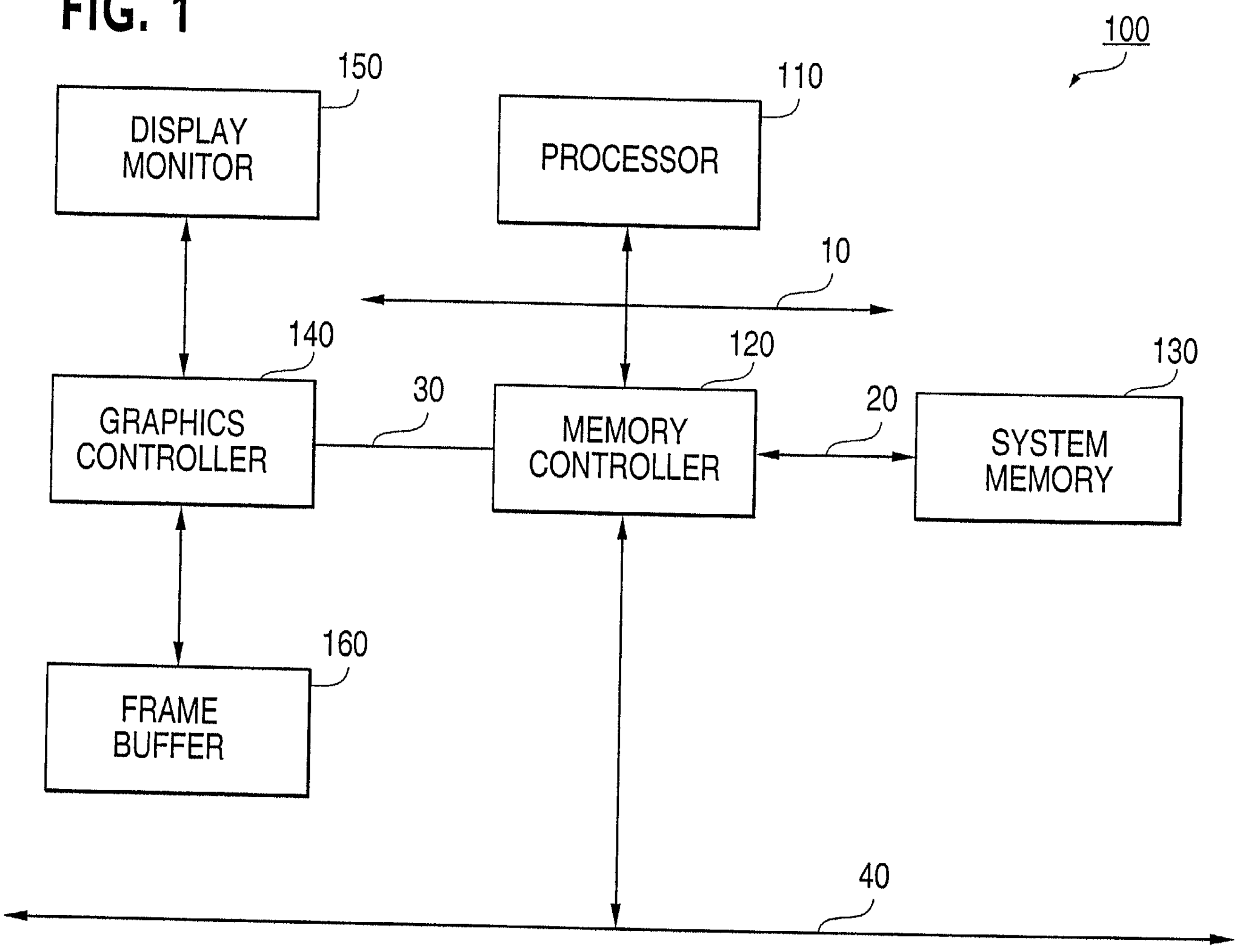

100
150
DISPLAY MONITOR
110
PROCESSOR
10
140
GRAPHICS CONTROLLER
30
120
MEMORY CONTROLLER
20
130
SYSTEM MEMORY
160
FRAME BUFFER
40

FIG. 2

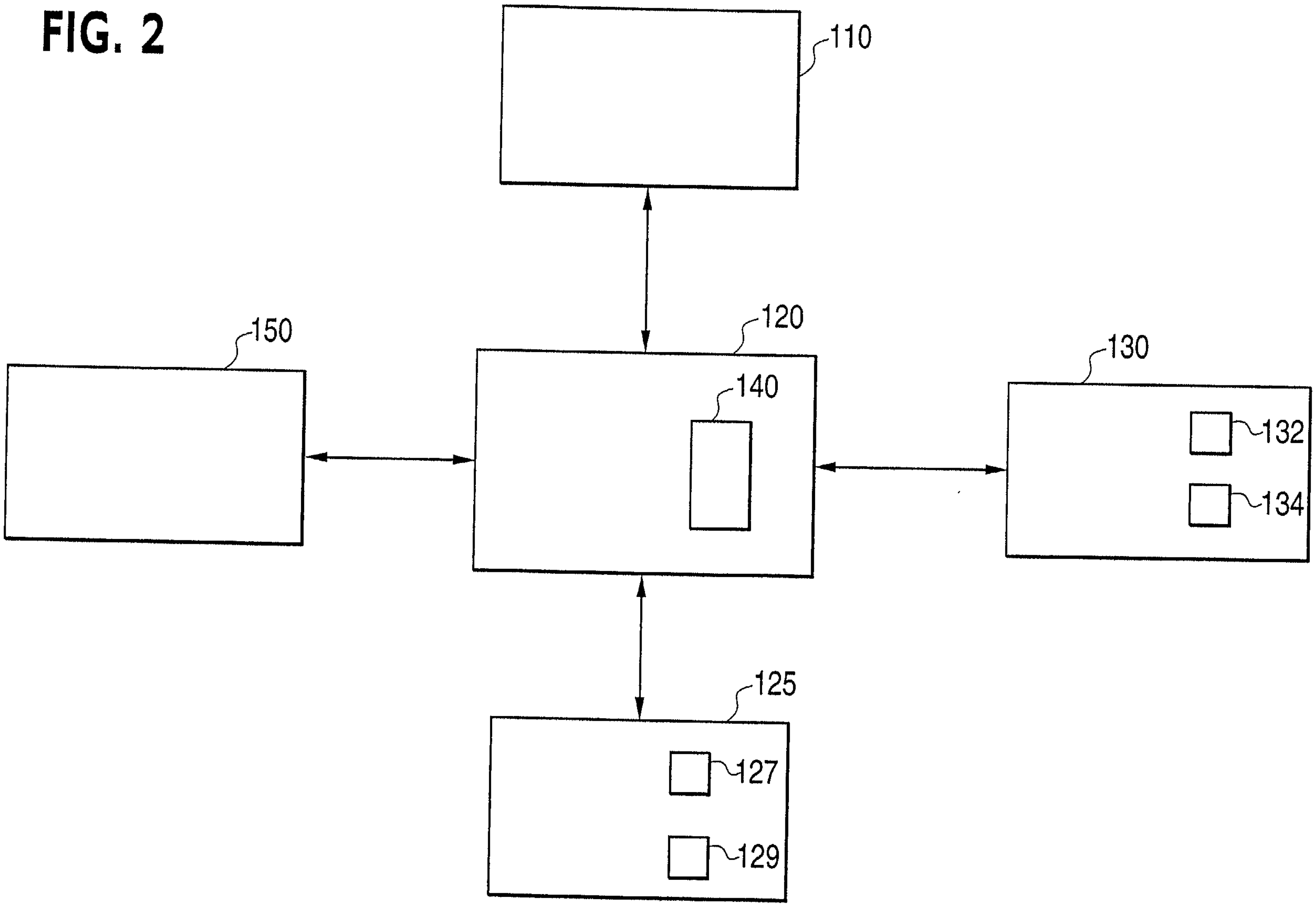


FIG. 3

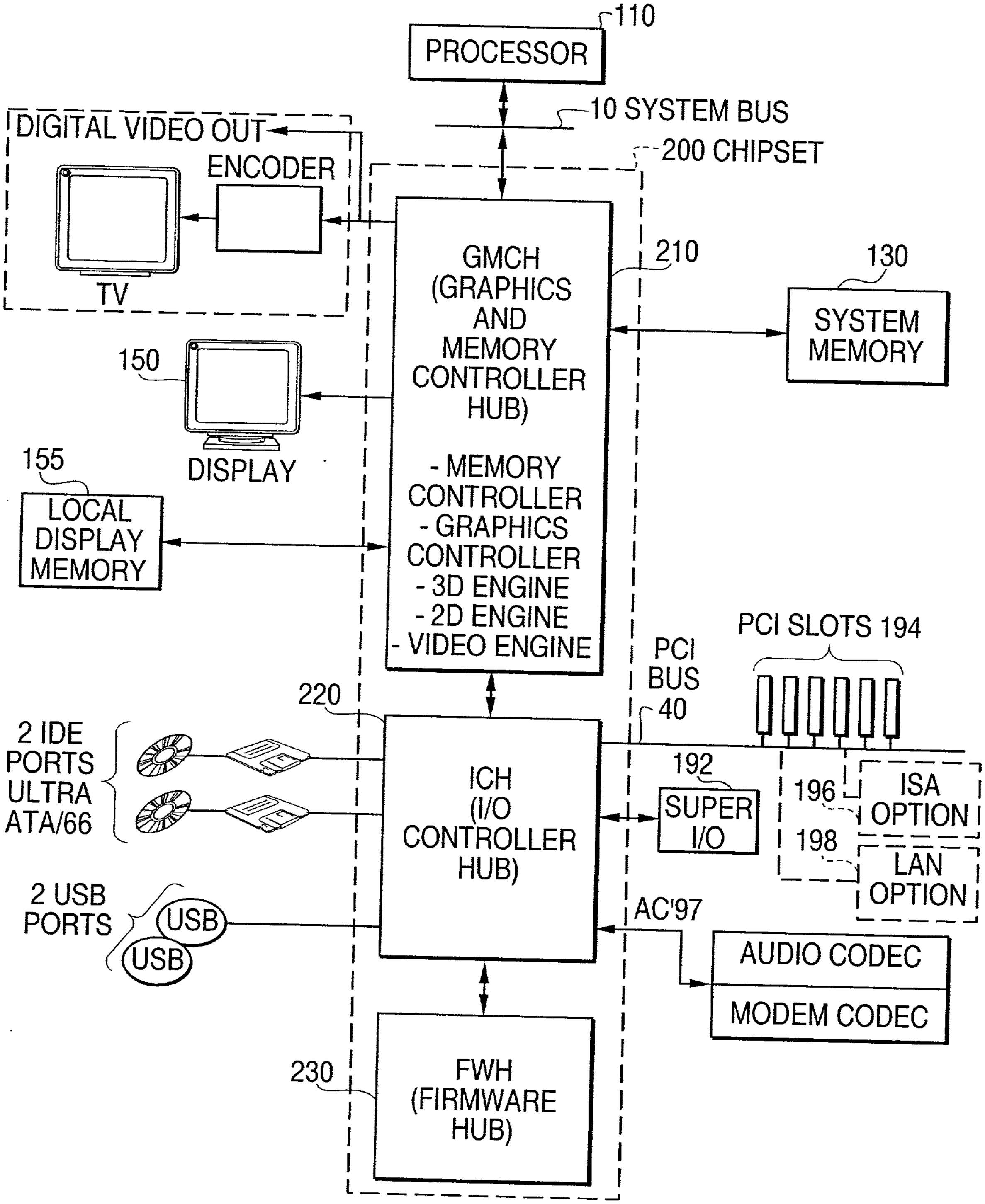

110
PROCESSOR
10 SYSTEM BUS
200 CHIPSET
DIGITAL VIDEO OUT
ENCODER
TV
210
GMCH (GRAPHICS AND MEMORY CONTROLLER HUB)
- MEMORY CONTROLLER
- GRAPHICS CONTROLLER
- 3D ENGINE
- 2D ENGINE
- VIDEO ENGINE
130
SYSTEM MEMORY
150
DISPLAY
155
LOCAL DISPLAY MEMORY
PCI SLOTS 194
PCI BUS 40
220
ICH (I/O CONTROLLER HUB)
2 IDE PORTS ULTRA ATA/66
192
SUPER I/O
196
ISA OPTION
198
LAN OPTION
2 USB PORTS
USB
USB
AC'97
AUDIO CODEC
MODEM CODEC
230
FWH (FIRMWARE HUB)

FIG. 4

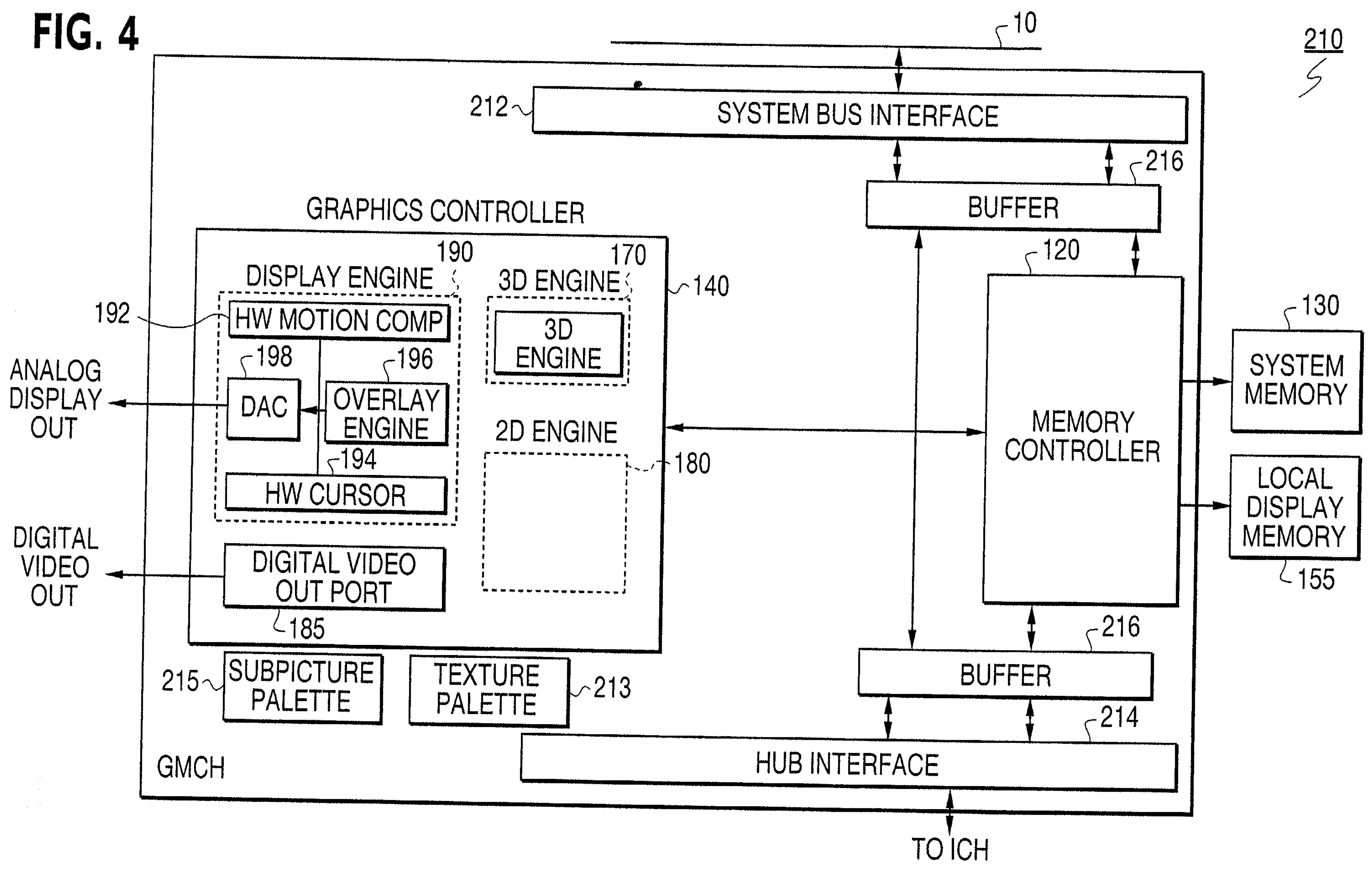

10
210
212
SYSTEM BUS INTERFACE
216
BUFFER
GRAPHICS CONTROLLER
190
DISPLAY ENGINE
170
3D ENGINE
140
120
192
HW MOTION COMP
3D ENGINE
130
SYSTEM MEMORY
198
196
ANALOG DISPLAY OUT
DAC
OVERLAY ENGINE
2D ENGINE
MEMORY CONTROLLER
194
180
HW CURSOR
LOCAL DISPLAY MEMORY
DIGITAL VIDEO OUT
DIGITAL VIDEO OUT PORT
155
185
216
BUFFER
215
SUBPICTURE PALETTE
TEXTURE PALETTE
213
214
GMCH
HUB INTERFACE
TO ICH

FIG. 5

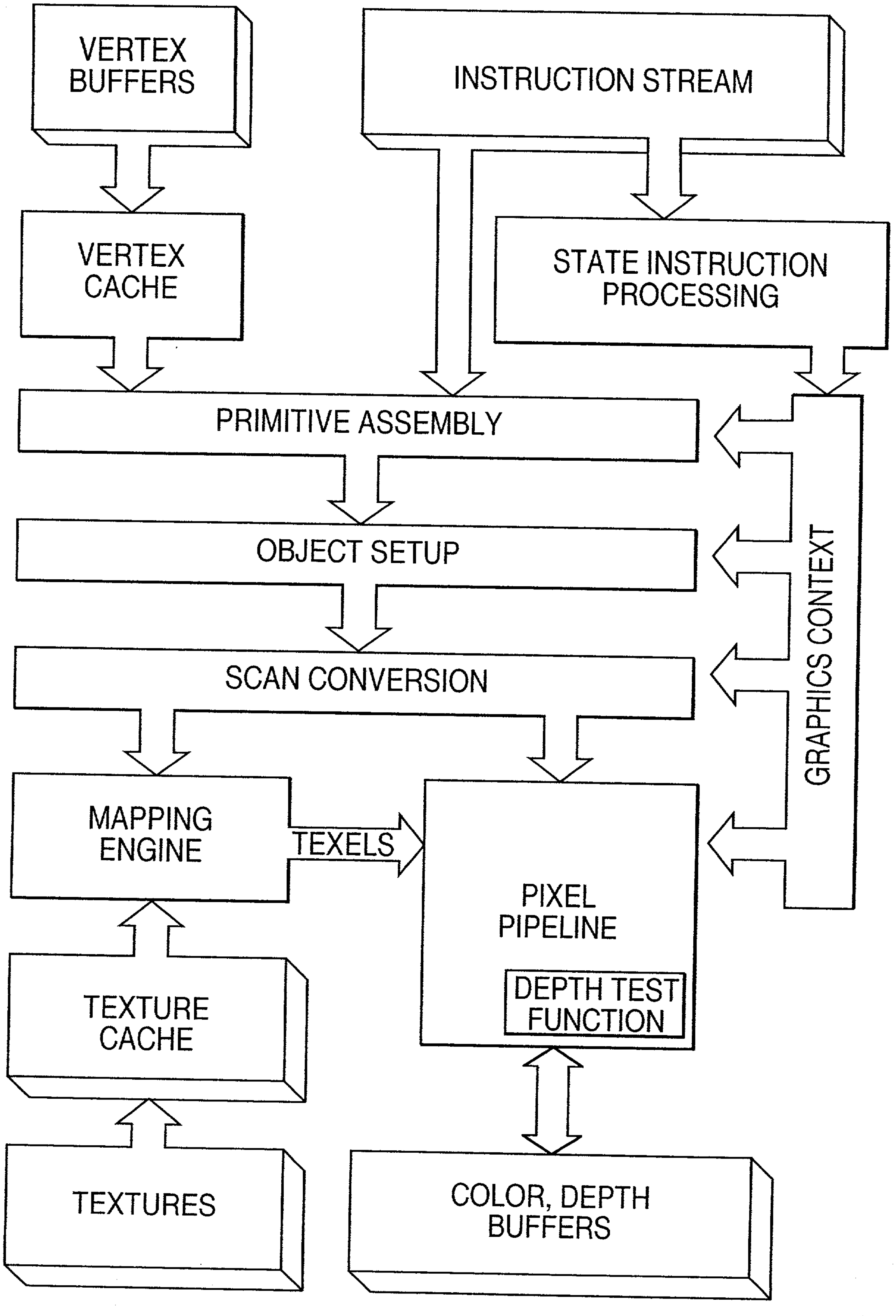

VERTEX BUFFERS
INSTRUCTION STREAM
VERTEX CACHE
STATE INSTRUCTION PROCESSING
PRIMITIVE ASSEMBLY
OBJECT SETUP
SCAN CONVERSION
GRAPHICS CONTEXT
MAPPING ENGINE
TEXELS
PIXEL PIPELINE
DEPTH TEST FUNCTION
TEXTURE CACHE
TEXTURES
COLOR, DEPTH BUFFERS

FIG. 6

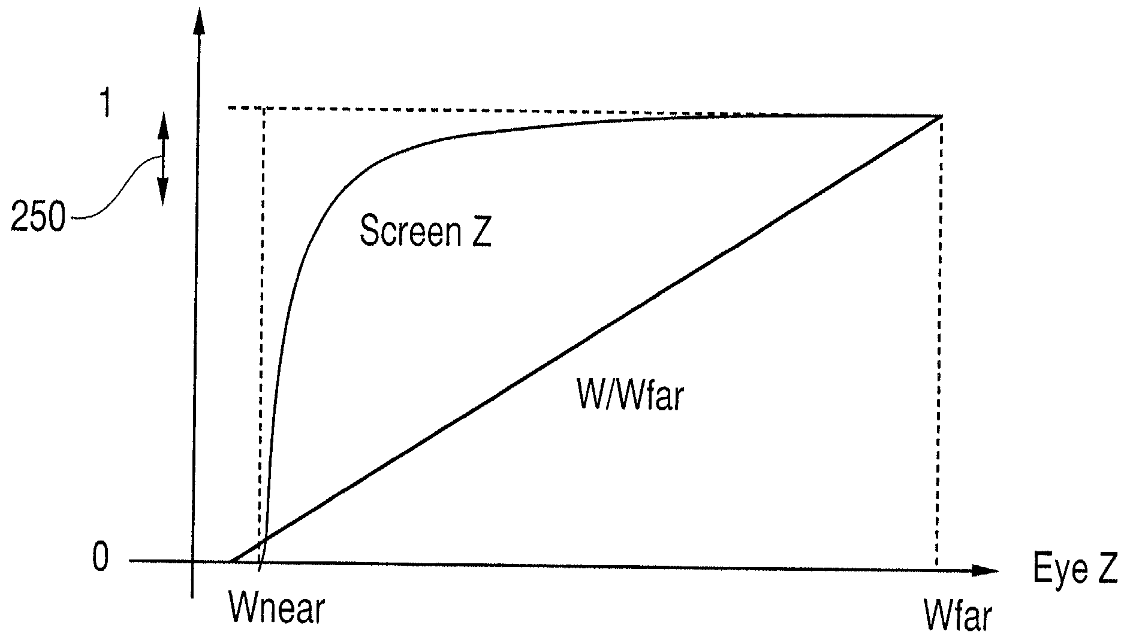


FIG. 7

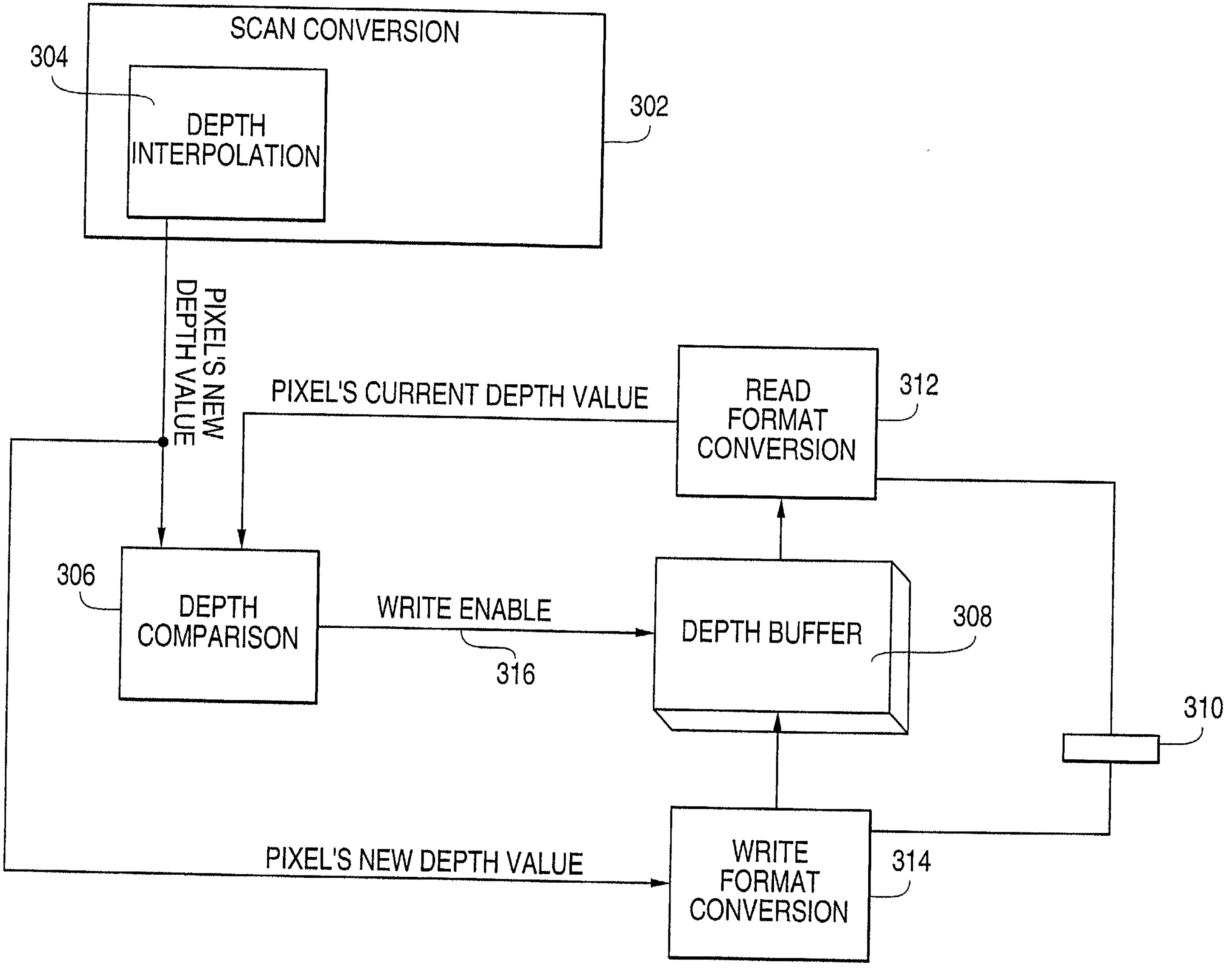
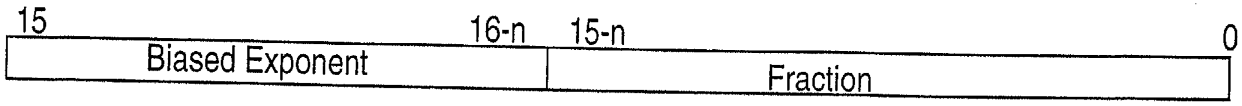
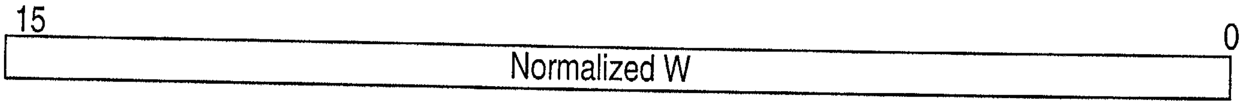

SCAN CONVERSION
304
DEPTH INTERPOLATION
302
PIXEL'S NEW DEPTH VALUE
PIXEL'S CURRENT DEPTH VALUE
READ FORMAT CONVERSION
312
306
DEPTH COMPARISON
WRITE ENABLE
316
DEPTH BUFFER
308
310
PIXEL'S NEW DEPTH VALUE
WRITE FORMAT CONVERSION
314

FIG. 8A



Bit	Description
15: 16-n	Biased Exponent: Format: n-bit unsigned biased exponent, where n= WExponentSelect. The exponent is biased by 2^n.
15-n:0	Fraction: Format: (16-n)-bit fractional portion of the floating point significand.

FIG. 8B



Bit	Description
15:0	Normalized W (W/Wfar): Format: U0.16 Range = [0, 1]

FIG. 8C

Biased Exponent (n bits)	Significand		Represented Value (W/WFar)
	Integer	Fraction	
exp = 0.2^n-1	1	frac	1.frac * 2^(exp-2^n)

FIG. 9A

31 24	23 24-n	23-n 0
Stencil	Biased Exponent	Fraction

Bit	Description
31:24	Stencil: Format: U8 Range = [0,255]
23:24-n	Biased Exponent: Format: n-bit unsigned biased exponent, where n= WExponentSelect. The exponent is biased by 2^n.
23-n:0	Fraction: Format: (16-n)-bit fractional portion of the floating point significand.

FIG. 9B

31 24	23 0
Stencil	Normalized W

Bit	Description
31:24	Stencil: Format: U8 Range = [0,255]
23:0	Normalized W (W/Wfar): Format: U0.24 Range = [0, 1]